AL8254 Core
Application Note

Rev. [6/2012]

6-19-2012

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General Information

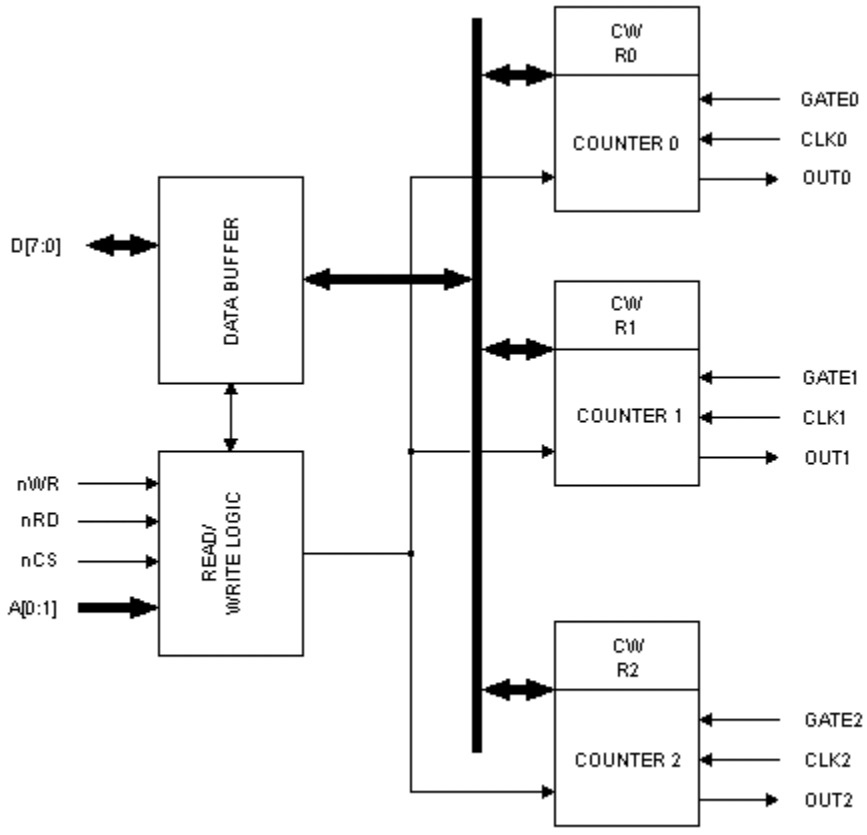
The AL8254 core is the VHDL model of the Intel™ programmable counter/timer device designed for use as an Intel microcomputer peripheral.

Features

- Functionally based on the Intel 8254 device
- Three Independent 16-Bit Counters
- Six Programmable Counter Modes
- Binary or BCD Counting

Block Diagram

The basic structure of the AL8254 core is shown below:



Contents

Behavioral

The behavioral model is designed for the functional simulation only and it cannot be synthesized or implemented into FPGAs. The behavioral model contains the following files:

- **AL8254.vhd** - the top level file of the AL8254 model

Synthesizable

See the Deliverables section of this document for further details.

Test Vectors

See the Deliverables section of this document for further details.

Interface

The pinout of the AL8254 core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in the table.

Port Name	Direction	Polarity	Description
DATA[7:0] 1)	INOUT		CPU data bus
nWR	IN	LOW	Write control
nRD	IN	LOW	Read control
nCS	IN	LOW	Chip select
A[0:1]	IN		Address bus
CLK0	IN		Clock for counter no 0
CLK1	IN		Clock for counter no 1
CLK2	IN		Clock for counter no 2
GATE0	IN		Gate input for counter 0
GATE1	IN		Gate input for counter 1
GATE2	IN		Gate input for counter 2
OUT0	OUT		Counter no 0 output
OUT1	OUT		Counter no 1 output
OUT2	OUT		Counter no 2 output

NOTES:

1. Each bidirectional pin is defined in the core interface as three separated VHDL ports. Optionally, using the VHDL Interface (See the Deliverables section of this document for further details), it can be merged to one bidirectional VHDL port.

Implementation Data

The core has been synthesized and implemented to different types of reprogrammable devices. The model has been verified using the simulation environment and tested using the real hardware.

Software				
Synthesis Tool	Synopsys FPGA Express™ build 2.1.3.3220			
Implementation Tools	Xilinx Foundation™ 2.1i SP2, Altera MAX+plusII™ 9.21, Quartus™ 1.0 A			
Verification Tool	Active-HDL™ 3.5 build 437			
Hardware				
Vendor	Xilinx		Altera	
Device Family	4K	Virtex™	FLEX™ 10K	APEX™ 20K
Target Device	XC4062XLA-9	XCV300-4	EPF10K100-1	APEX20
Area	304CLBs(13%)	372Slices(12%)	soon come	soon come
System Clock fmax	28MHz	40MHz	soon come	soon come

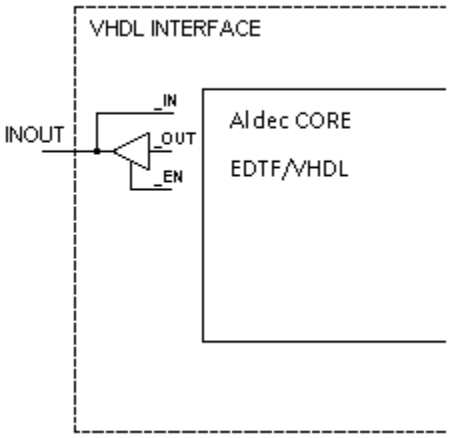
Deliverables

After you request the desired compiled synthesizable core, Aldec delivers the following files:

- Both technology-dependent EDIF (AL8254_CORE.EDN) and VHDL (AL8254_CORE.VHD) netlists
- Aldec VHDL Interface (AL8254.VHD)
- Application Notes
- Testbench example

Usually Aldec delivers both EDIF and VHDL netlists for customers who order the synthesizable model. The EDIF netlist is used for the place and route process and VHDL is the post-synthesis netlist used for the simulation only. Of course, both netlists are technology-dependent, because they are created after the synthesis where the customer needs to specify a vendor, target family, etc.

Aldec provides optionally a VHDL interface for its synthesizable models for these customers who need bidirectional ports in the core interface. See the picture below:



Aldec provides also a set of VHDL test benches for their cores. Usually they are sold at the additional charge.

Source codes are sold on a case-by-case basis.